WHAT IS CLAIMED IS:

1. A squeezable tail current source, comprising:

a first transistor pair that replicates a main input transistor pair of a differential amplifier circuit, wherein both the first transistor pair and the main input transistor pair receive a common voltage input at their respective gates;

a second transistor pair;

a bias transistor;

a first current source;

a folding transistor; and

a second current source that biases the folding transistor,

wherein the first transistor pair, the second transistor pair, the bias transistor, and the first current source are configured such that current through the main input transistor pair is maintained as the common voltage input varies; and

wherein the second current source and the folding transistor isolate the bias transistor and the second transistor pair from a drain voltage of the first transistor pair, thereby causing the first transistor pair and the main input transistor pair to have a common drain bias.

2. The squeezable tail current source of claim 1, wherein current through the second transistor pair and the bias transistor is squeezed as the common voltage input is decreased, thereby increasing a gate voltage of the bias transistor, and thereby causing current through both the first transistor pair and the main input transistor pair to remain nearly constant.

3. The squeezable tail current source of claim 1, wherein:

the first transistor pair has a common source and a common drain;

the second transistor pair has a common source, a common drain, and a common gate, wherein the second transistor pair common drain is coupled to a common source of the main input transistor pair;

the bias transistor has a drain coupled to the first transistor pair common source, a source coupled to the second transistor pair common source, and a gate coupled to the second transistor pair common gate;

the first current source has an output coupled to the first transistor pair common drain;

the second current source has an input coupled to the bias transistor gate and an output coupled to the bias transistor source; and

the folding transistor has a source coupled to the first transistor pair common drain, a drain coupled to the bias transistor gate, and a gate that has a voltage bias common to a common gate of a third transistor pair of the differential amplifier circuit, wherein respective sources of the third transistor pair are coupled to respective drains of the main input transistor pair.

4. The squeezable tail current source of claim 3, wherein:

the first transistor pair, the second transistor pair, and the bias transistor are NMOS transistors; and

the folding transistor is a PMOS transistor.

5. The squeezable tail current source of claim 1, wherein:

the first transistor pair, the second transistor pair, and the bias transistor are PMOS transistors; and

the folding transistor is an NMOS transistor.

6. A differential input buffer, comprising:

a first main input transistor pair;

a second main input transistor pair;

a first replica transistor pair that replicates the first main input transistor pair, wherein both the first replica transistor pair and the first main input transistor pair receive a first common voltage input at their respective gates;

a second replica transistor pair that replicates the second main input transistor pair, wherein both the second replica transistor pair and the second main input transistor pair receive a second common voltage input at their respective gates;

a first tail transistor pair;

a second tail transistor pair;

a first bias transistor;

a second bias transistor;

a first current source;

a second current source;

a first folding transistor;

a second folding transistor;

a first biasing current source that biases the first folding transistor; and

a second biasing current source that biases the second folding transistor,

wherein the first main input transistor pair, the first replica transistor pair, the first tail transistor pair, the first bias transistor, and the first current source are configured such that current through the first main input transistor pair is maintained as the first common voltage input to the first main input pair varies;

wherein the second main input transistor pair, the second replica transistor pair, the second tail transistor pair, the second bias transistor, and the second current source are configured such that current through the second

main input transistor pair is maintained as the second common voltage input to the second main input pair varies;

wherein the first biasing current source and the first folding transistor isolate the first bias transistor and the first tail transistor pair from a drain voltage of the first replica transistor pair, thereby causing the first replica transistor pair and the first main input transistor pair to have a common drain bias; and

wherein the second biasing current source and the second folding transistor isolate the second bias transistor and the second tail transistor pair from a drain voltage of the second replica transistor pair, thereby causing the second replica transistor pair and the second main input transistor pair to have a common drain bias.

7. The differential input buffer of claim 6, wherein:

current through the first tail transistor pair and the first bias transistor is squeezed as the first common voltage input to the first main input transistor pair is decreased, thereby increasing a gate voltage of the first bias transistor, and thereby causing current through both the first replica transistor pair and the first main input transistor pair to remain nearly constant; and

current through the second tail transistor pair and the second bias transistor is squeezed as the second common voltage input to the second main input transistor pair is decreased, thereby increasing a gate voltage of the second bias transistor, and thereby causing current through both the second replica transistor pair and the second main input transistor pair to remain nearly constant.

8. The differential input buffer of claim 6, wherein:

the first main input transistor pair has a common source;

the second main input transistor pair has a common source;

the first replica transistor pair has a common source and a common drain;

the second replica transistor pair has a common source and a common drain;

the first tail transistor pair has a common source, a common drain, and a common gate, wherein the first tail transistor pair common drain is coupled to the first main input transistor pair common source;

the second tail transistor pair has a common source, a common drain, and a common gate, wherein the second tail transistor pair common drain is coupled to the second main input transistor pair common source;

the first bias transistor has a drain coupled to the first replica transistor pair common source, a source coupled to the first tail transistor pair common source, and a gate coupled to the first tail transistor pair common gate;

the second bias transistor has a drain coupled to the second replica transistor pair common source, a source coupled to the second tail transistor pair common source, and a gate coupled to the second tail transistor pair common gate;

the first current source has in output coupled to the first replica transistor pair common drain;

the second current source has an output coupled to the second replica transistor pair common drain;

the first biasing current source has an input coupled to the first bias transistor gate and an output coupled to the first bias transistor source;

the second biasing current source has an input coupled to the second bias transistor gate and an output coupled to the second bias transistor source;

the first folding transistor has a source coupled to the first replica transistor pair common drain, a drain coupled to the first bias transistor gate, and a gate that has a voltage bias common to a common gate of a bias-sharing

transistor pair, wherein respective sources of the bias-sharing transistor pair are coupled to respective drains of the first main input transistor pair; and

the second folding transistor has a source coupled to the second replica transistor pair common drain, a drain coupled to the second bias transistor gate, and a gate that has a voltage bias common to the common gate of the bias-sharing transistor pair, wherein respective sources of the bias-sharing transistor pair are coupled to respective drains of the second main input transistor pair.

9. The differential input buffer of claim 8, wherein:

the first main input transistor pair, the second main input transistor pair, the first replica transistor pair, the second replica transistor pair, the first tail transistor pair, the second tail transistor pair, the first bias transistor, and the second bias transistor are NMOS transistors; and

the first folding transistor and the second folding transistor are PMOS transistors.

10. The differential input buffer of claim 6, wherein:

the first main input transistor pair, the second main input transistor pair, the first replica transistor pair, the second replica transistor pair, the first tail transistor pair, the second tail transistor pair, the first bias transistor, and the second bias transistor are PMOS transistors; and

the first folding transistor and the second folding transistor are NMOS transistors.

11. The differential input buffer of claim 6, further comprising:

a first stage having an input coupled to drains of the first and second main input transistor pairs and having an output; and

a second stage having an input coupled to the first stage output and having an output coupled to an output of the differential input buffer.

12. A method of regulating current through a main input differential pair of a differential amplifier circuit while maintaining high linearity, the method comprising:

providing a voltage input to the main input differential pair;

mirroring a tail current to that of the current through the main input differential pair by using a squeezable tail current source that includes

a current source;

a first transistor pair;

a bias transistor; and

a second transistor pair;

isolating the bias transistor and the first transistor pair from a drain voltage of the second transistor pair, thereby causing the second transistor pair and the main input transistor pair to have a common drain bias; and

squeezing the tail current as the voltage input is decreased, thereby increasing a gate voltage of the bias transistor and allowing current through the main input differential pair to remain nearly constant.

13. The method of regulating current of claim 12, wherein the mirroring step uses a squeezable tail current source in which:

the first transistor pair has a common drain coupled to a main input differential pair common source;

the bias transistor has a source coupled to a first transistor pair common source and a gate coupled to a first transistor pair common gate; and

the second transistor pair has a common source coupled to a bias transistor drain, a common drain coupled to an output of the current source, and a pair of gates with common voltage inputs as those of respective gates of the main input transistor pair.

14. The method of regulating current of claim 13, wherein the isolating step is accomplished by including in the squeezable tail current source:

a biasing current source having an input coupled to the bias transistor gate and an output coupled to the bias transistor source; and

a folding transistor having a source coupled to the second transistor pair common drain, a drain coupled to the bias transistor gate, and a gate that has a voltage bias common to a common gate of a bias-sharing transistor pair, wherein respective sources of the bias-sharing transistor pair are coupled to respective drains of the main input transistor pair.